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a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion; and

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode as seen in plan view, said side wall being formed of a lamination of at least two insulation films having different etching properties, and wherein said insulation films contact each other.--

REMARKS

Claims 1, 2 and 3 have been amended to further define the invention over the prior art. Claims 11, 12 and 13 have been amended to reflect the changes in claims 1, 2 and 3. New claims 21-23 have been added to further scope the invention.

Pursuant to 37 CFR § 1.121, a marked copy of the amended claims showing the changes made therein accompanies this Amendment. No new matter has been entered.

Turning to the rejection of claims 1, 3, 4, 6, 7, 9, 11, 13, 14 and 16 under 35 USC § 102(b) as being anticipated by Iguchi et al., U.S. Patent No. 5,734,185, claims 1 and 3 have been amended to include the feature that the two insulation films forming the side walls are in contact with the interlayer insulation film and the gate electrode. Iguchi et al. does not teach this feature. Iguchi et al. teaches a side wall 16 with three insulation films 16a, 15, 3 and 2, where only four of the films contact the gate electrode and the interlayer insulation film (Figures 1 and 16). Iguchi et al. does not teach a sidewall having more than one layer, where each layer touches both the gate electrode and the interlayer insulation film. Thus, Iguchi et al. cannot anticipate this new aspect of claims 1 and 3, nor any claims dependent therefrom.

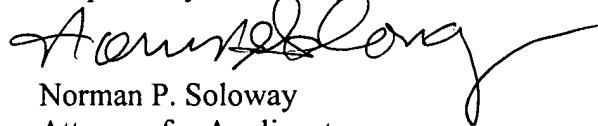
Turning to the rejection of claims 2, 5, 8, 10, 12 and 15 under 35 USC § 103(a) as being unpatentable over Iguchi et al. as applied to claims 1, 3, 4, 6, 7, 9, 11, 13, 14 and 16 in view of Kim, U.S. Patent No. 6,204,538, claim 2 similarly has been amended to require that the side walls are formed of two insulation films that are both in contact with the interlayer insulation film and said gate electrode. As noted above, this feature is not described in Iguchi et al. Further, Kim does not teach this either. Kim teaches a single gate insulating film formed underneath the electrode. (Figure 4C). Kim does not teach a side wall formed on a side surface of the gate electrode that is covered by a visor portion and is comprised of two insulation films in contact with both the gate electrode and the interlayer insulation film. Thus, no combination of Iguchi et al. and Kim could achieve or render obvious claim 2 or any claims dependent therefrom.

A credit card payment Form PTO-2038 authorizing a charge of \$1,002.00 covering the RCE fee and \$252.00 fee for payment of the added independent claims, accompanies this Amendment.

Having dealt with all of the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account No. 08-1391.

Respectfully submitted,



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Amendment C with RCE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on March 27, 2003, at Tucson, Arizona.

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MARKED AMENDED CLAIMS

SERIAL NO. 10/036,955

DOCKET NO. NEC 01FN061



MARKED CLAIMS SHOWING CHANGES MADE

1. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode as seen in plan view; and

an interlayer insulation film covering said gate electrode and being in contact with said side wall,

wherein said sidewall is formed of at least two insulation films, and each of said insulation films contacts both said interlayer insulation film and said gate electrode.

2. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode as seen in plan view;

an interlayer insulation film covering said gate electrode; and

a contact formed in said interlayer insulation film and being in contact with said side wall,

wherein said sidewall is formed of at least two insulation films, and each of said insulation films contacts both said interlayer insulation film and said gate electrode.

3. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on said semiconductor substrate;

a gate electrode formed on said gate insulation film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion; and

a side wall formed on a side surface of said gate electrode so as to be covered behind a visor portion of said gate electrode as seen in plan view, said side wall being formed of a lamination of at least two insulation films having different etching properties, each of said insulation films contacts both said interlayer insulation film and said gate electrode.

11. (Twice Amended) The semiconductor device according to claim 4, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part [and is formed out of at least two different insulation films].

12. (Twice Amended) The semiconductor device according to claim 5, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part [and is formed out of at least two different insulation films].

13. (Twice Amended) The semiconductor device according to claim 6, wherein said side wall is formed on both a side surface of said upper part and a side surface of said lower part [and is formed out of at least two different insulation films].